difference in field plate length.

- 20. (New) The device of claim 19, where the first portion is an SOI- LDMOS device.
- 21. (New) The device of claim 20, where the SOI-LDMOS device is any of an NMOS or

PMOS device.

REMARKS

The subject Office Action allowed claims 15 and 16 and objected to claims 7 and 8 as being dependent from a rejected base claim. Claims 1-3, 6 and 9 stand rejected under 35 USC §102 as being anticipated by Williams et al., US Patent No. 5,818,084 and by Kikuchi et al., Japan Patent No. JP 51-147972. Claims 10-14, 17 and 18 were previously withdrawn as non-elected.

In response to the §102 rejections, claim 1 has been amended to more clearly and precisely claim the invention. As amended, claim 1 requires that the "second portion [being] is less resistant to breakdown voltage and able to survive breakdown without device failure." This language is supported in the specification in the top paragraph of page 3.

Whereas the Office Action states that the hybrid semiconductor devices of Williams et al. and of Kikuchi et al. inherently allow breakdown to occur at higher voltage in a first portion and at lower voltage in a second portion, the present invention discloses and claims a further attribute: that the device maintains its ability to function beyond breakdown, i.e. "survives breakdown without device failure." Such a feature is not

Serial No. 09/894.083 Attorney Ref: US010320

disclosed in any of the known prior art. It is thus submitted that claim 1 as amended is allowable over the cited references. The limitations of claims 2 and 3 are incorporated int amended claim 1 and claims 2 and 3 are cancelled hereby. Claims 6 - 9, being

dependent upon claim 1 are thus also believed to be allowable.

New claim 19 incorporates the allowable combined limitations of claims 6 and 7 with original claim 1, and is thus stated to be allowable. New claims 20 and 21, dependent upon claim 19 are also submitted as being allowable.

It is respectfully submitted that the additional cited prior art is not a barrier to allowance

A marked-up copy of amended claim 1, showing the changes, is appended hereto.

In view of the foregoing amendment and remarks, it is respectfully submitted that all claims pending are allowable. Therefore, reconsideration and allowance are respectfully requested.

Respectfully submitted

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal service as first class mail, in a postage prepaid envelope, addressed to Box Non-Fee Amendments, Cormissioner for Patents, Washington, D.C. 20231 on 19 fee 2003.

MARKED UP VERSION SHOWING CHANGES TO CLAIM 1:

- 1. (Twice Amended) A hybrid semiconductor device, comprising:
 - a first portion being relatively resistant to breakdown voltage, the first portion comprising a MOS transistor; and

a second portion being less resistant to breakdown voltage and able to survive breakdown without device failure, the second portion residing adjacent the first portion and comprising a diode, wherein the diode has an identical structure as the MOS transistor, except for a source region.